

REMARKS

The Office Action dated December 22, 2004, has been received and carefully considered. In this response, claims 1-4, 8, 11, and 16-22 have been amended. Entry of the amendments to claims 1-4, 8, 11, and 16-22 is respectfully requested. Reconsideration of the outstanding rejections in the present application is also respectfully requested based on the following remarks.

At the outset, Applicants note with appreciation the indication on page 5 of the Office Action that claims 21 and 22 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicants have opted to defer rewriting claims 21 and 22 in independent form pending reconsideration of the arguments presented below with respect to the rejected claims.

I. THE ANTICIPATION REJECTION OF CLAIMS 1-4, 8-11, AND 16-20

On pages 2-5 of the Office Action, claims 1-4, 8-11, and 16-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Goldrain (U.S. Patent No. 5,742,798). This rejection is hereby respectfully traversed with amendment.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id.

Regarding claim 1, the Examiner asserts that Goldrain discloses the claimed invention. However, it is respectfully submitted that Goldrain fails to disclose a method for accommodating transition-induced delay comprising: determining a first relationship between a current logic state and a next logic state of a first data signal; and adjusting a first delay of the first data signal based at least in part upon the first

relationship by controlling at least one delay element, as presently claimed. Indeed, Goldrain is specifically directed to the synchronization of clock signals. In contrast, claim 1 sets forth a method for accommodating transition-induced delay in data signals. Also, Goldrain only discloses detecting the state of a delayed clock signal (511) on the rising edge of a reference clock signal (515) (see column 4, lines 46-48). However, this does not amount to determining a first relationship between a current logic state and a next logic state of a first data signal, as presently claimed. Further, Goldrain only discloses determining the number of elementary delays (502) that are required to cause a delay of half a clock cycle of a clock signal (see column 5, lines 4-12). However, this does not amount to adjusting a first delay of the first data signal based at least in part upon the first relationship by controlling at least one delay element, as presently claimed. Thus, it is respectfully submitted that Goldrain does not claim, disclose, or even suggest the claimed invention. Accordingly, it is respectfully submitted that claim 1 should be allowable.

Claims 2-4 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-4 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims

recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 2 recites determining a second relationship between a current logic state and a next logic state of a second data signal, wherein the step of adjusting the first delay of the first data signal based at least in part upon the first relationship further comprises adjusting the first delay of the first data signal based at least in part upon the first and second relationships. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature. Also, claim 3 recites that the step of adjusting the first delay of the first data signal based at least in part upon the first and second relationships further comprises adjusting the first delay of the first data signal and a second delay of the second data signal based at least in part upon the first and second relationships. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature. Furthermore, claim 4 recites that the step of adjusting the first delay of the first data signal based at least in part upon the first relationship further comprises providing less delay when the current logic state and the next logic state of the first data signal are different than when the current logic state and the next logic state of the first data signal are similar. Nowhere does Goldrain claim, disclose, or

even suggest this claimed feature.

Regarding claim 8, the Examiner asserts that Goldrain discloses the claimed invention. However, it is respectfully submitted that Goldrain fails to disclose an apparatus for accommodating transition-induced delay comprising: a transition detection block having a plurality of inputs for receiving a corresponding plurality of data signals, the transition detection block detecting transitions of the plurality of data signals; and a delay adjustment block coupled to the transition detection block, the delay adjustment block adjusting a delay in at least one of the plurality of data signals by controlling at least one delay element, as presently claimed. Indeed, Goldrain is specifically directed to the synchronization of clock signals. In contrast, claim 1 sets forth an apparatus for accommodating transition-induced delay in data signals. Also, Goldrain only discloses detecting the state of a delayed clock signal (511) on the rising edge of a reference clock signal (515) (see column 4, lines 46-48). However, this does not amount to a transition detection block having a plurality of inputs for receiving a corresponding plurality of data signals, wherein the transition detection block detects transitions of the plurality of data signals, as presently claimed. Further, Goldrain only discloses determining the number of elementary

delays (502) that are required to cause a delay of half a clock cycle of a clock signal (see column 5, lines 4-12). However, this does not amount to a delay adjustment block coupled to the transition detection block, wherein the delay adjustment block adjusts a delay in at least one of the plurality of data signals by controlling at least one delay element, as presently claimed. Thus, it is respectfully submitted that Goldrain does not claim, disclose, or even suggest the claimed invention. Accordingly, it is respectfully submitted that claim 8 should be allowable.

Claims 9-11 are dependent upon independent claim 8. Thus, since independent claim 8 should be allowable as discussed above, claims 9-11 should also be allowable at least by virtue of their dependency on independent claim 8. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 9 recites that the transition detection block detects a first type of the transitions from a first level to a second level and a second type of the transitions from the second level to the first level. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature with respect to data signals. Also, claim 10 recites that the delay adjustment block adjusts the delay based on a relationship between the first type of the

transitions and the second type of the transitions. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature with respect to data signals. Further, claim 11 recites that the relationship is a difference between a first number of the plurality of data signals exhibiting the first type of the transitions and a second number of the plurality of data signals exhibiting the second type of the transitions. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature.

Regarding claim 16, the Examiner asserts that Goldrain discloses the claimed invention for the same reasons that Goldrain discloses the invention recited in claim 8. However, for the same reasons as discussed above for claim 8, it is respectfully submitted that Goldrain fails to disclose a method for accommodating transition-induced delay comprising: detecting transitions of a plurality of data signals; and adjusting a delay of at least one of the plurality of data signals based at least in part upon the transitions of the plurality of data signals by controlling at least one delay element, as presently claimed. Thus, it is respectfully submitted that Goldrain does not claim, disclose, or even suggest the claimed invention. Accordingly, it is respectfully submitted that claim 16 should be allowable.

Claims 17-22 are dependent upon independent claim 16.

Thus, since independent claim 16 should be allowable as discussed above, claims 17-22 should also be allowable at least by virtue of their dependency on independent claim 16. Moreover, similar to claims 9-11, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-4, 8-11, and 16-20 be withdrawn.

II. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to

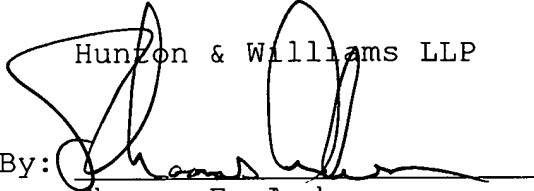
Patent Application
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Deposit Account No. 50-0206, and please credit any excess fees
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APPENDIX A

1 (Currently Amended). A method for accommodating transition-induced delay comprising the steps of:

determining a first relationship between a ~~first-line~~ current logic state ~~of a first line~~ and a ~~first-line~~ next logic state of a first data signal; and

adjusting a first delay ~~in the first line~~ of the first data signal based at least in part upon the first relationship by controlling ~~a delay time of~~ at least one delay element.

2 (Currently Amended). The method of claim 1 further comprising the step of:

determining a second relationship between a ~~second-line~~ current logic state ~~of a second line~~ and a ~~second-line~~ next logic state of a second data signal, wherein the step of adjusting the first delay ~~in the first line~~ of the first data signal based at least in part upon the first relationship further comprises the step of:

adjusting the first delay ~~in the first line~~ of the first data signal based at least in part upon the first and second relationships.

3 (Currently Amended). The method of claim 2, wherein the step

of adjusting the first delay ~~in the first line~~ of the first data signal based at least in part upon the first and second relationships further comprises the step of:

adjusting the first delay ~~in the first line~~ of the first data signal and a second delay ~~in the second line~~ of the second data signal based at least in part upon the first and second relationships.

4 (Currently Amended). The method of claim 1, wherein the step of adjusting the first delay ~~in the first line~~ of the first data signal based at least in part upon the first relationship further comprises the step of:

providing less delay when the ~~first line~~ current logic state and the ~~first line~~ next logic state of the first data signal are different than when the ~~first line~~ current logic state and the ~~first line~~ next logic state of the first data signal are similar.

5-7 (Cancelled).

8 (Currently Amended). An apparatus for accommodating transition-induced delay comprising:

a transition detection block having a plurality of inputs,

~~the inputs coupled to a~~ for receiving a corresponding plurality of lines data signals, the transition detection block detecting transitions of the ~~lines~~ plurality of data signals; and

a delay adjustment block coupled to the transition detection block, the delay adjustment block adjusting a delay in at least one of the ~~lines~~ plurality of data signals by controlling ~~a delay time of~~ at least one delay element.

9 (Original). The apparatus of claim 8, wherein the transition detection block detects a first type of the transitions from a first level to a second level and a second type of the transitions from the second level to the first level.

10 (Original). The apparatus of claim 9, wherein the delay adjustment block adjusts the delay based on a relationship between the first type of the transitions and the second type of the transitions.

11 (Currently Amended). The apparatus of claim 10, wherein the relationship is a difference between a first number of the ~~lines~~ plurality of data signals exhibiting the first type of the transitions and a second number of the ~~lines~~ plurality of data signals exhibiting the second type of the transitions.

12-15 (Cancelled).

16 (Currently Amended). A method for accommodating transition-induced delay comprising the steps of:

detecting transitions ~~on~~ of a plurality of ~~lines~~ data signals; and

adjusting a delay ~~in~~ of at least one of the plurality of ~~lines~~ data signals based at least in part upon the transitions ~~on~~ of the plurality of ~~lines~~ data signals by controlling a ~~delay time of~~ at least one delay element.

17 (Currently Amended). The method of claim 16, wherein the step of detecting transitions ~~on~~ of the plurality of ~~lines~~ data signals further comprises the steps of:

detecting first-level-to-second-level transitions ~~on~~ of the plurality of ~~lines~~ data signals; and

detecting second-level-to-first-level transitions ~~on~~ of the plurality of ~~lines~~ data signals.

18 (Currently Amended). The method of claim 17, wherein the step of adjusting the delay ~~in~~ of the at least one of the plurality of ~~lines~~ data signals based at least in part upon the

transitions ~~on~~ of the plurality of ~~lines~~ data signals further comprises the step of:

adjusting the delay ~~in~~ of the at least one of the plurality of ~~lines~~ data signals based at least in part upon a difference in respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions.

19 (Currently Amended). The method of claim 18, wherein the step of adjusting the delay ~~in~~ of the at least one of the plurality of ~~lines~~ data signals based at least in part upon the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions further comprises the step of:

increasing the delay when the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions is decreased.

20 (Currently Amended). The method of claim 18, wherein the step of adjusting the delay ~~in~~ of the at least one of the plurality of ~~lines~~ data signals based at least in part upon the difference in respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions further comprises the step of:

adjusting the delay differently when there are more of the first-level-to-second-level transitions than when there are more of the second-level-to-first-level transitions.

21 (Currently Amended). The method of claim 18, wherein the step of adjusting the delay ~~in~~ of the at least one of the plurality of ~~lines~~ data signals based at least in part upon the difference in respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions further comprises the step of:

adjusting the delay ~~in~~ of the at least one of the plurality of ~~lines~~ data signals based at least in part upon a comparison of the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions to a threshold.

22 (Currently Amended). The method of claim 21, wherein the step of adjusting the delay ~~in~~ of the at least one of the plurality of ~~lines~~ data signals based at least in part upon the comparison of the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions to the threshold further comprises the step of:

adjusting the delay ~~in~~ of the at least one of the plurality

of ~~lines~~ data signals based at least in part upon a comparison of the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions to a plurality of thresholds, with the delay adjusted a different amount for a first threshold of the plurality of thresholds than for a second threshold of the plurality of thresholds.

23-52 (Cancelled).